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Title: **METHODS FOR FABRICATING GIANT MAGNETORESISTIVE (GMR) DEVICES**

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GOVERNMENT RIGHTS

The United States Government has acquired certain rights in this invention pursuant to Contract No. DTRA01-00-C-0002 awarded by DTRA.

BACKGROUND

1. Field

The present invention relates generally to magnetoresistive devices and, more particularly, to improved methods for fabricating giant magnetoresistive devices, e.g., for magnetic memories.

2. Related Art

The discovery of the giant magnetoresistive (GMR) effect has led to the development of a number of spin-based electronic devices. The GMR effect is observed in certain thin-film devices that are made up of alternating ferromagnetic and nonmagnetic layers. The resistance of a GMR device is lowest when the magnetic moments of the ferromagnetic layers are in a parallel orientation, and the resistance is highest when the magnetic moments are in an antiparallel orientation.

One type of GMR device is commonly referred to as a "spin valve." A spin valve typically includes two ferromagnetic layers that are separated by a thin layer of a non-magnetic metal, such as copper, and also includes an antiferromagnetic layer that "pins" the magnetization of one of the ferromagnetic layers. Thus, the magnetization of the

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"pinned" ferromagnetic layer remains generally fixed when moderate magnetic fields are applied. In contrast, the magnetization of the other ferromagnetic layer is relatively "free." Thus, by applying an appropriate magnetic field, the magnetization of the free ferromagnetic layer can be switched while the magnetization of the pinned ferromagnetic layer is unchanged. In this way, applied magnetic fields can change the relative orientations of the magnetizations in the ferromagnetic layers, which, in turn, can be detected as a change in resistance. In particular, the resistance of spin valve 10 is typically lowest when the magnetizations of the ferromagnetic layers are in a parallel orientation and highest when the magnetizations are in an antiparallel orientation.

Another type of GMR device is commonly referred to as a "pseudo spin valve." Like a spin valve, a pseudo spin valve typically includes two ferromagnetic layers that are separated by a layer of a nonmagnetic metal, with the magnetization of one of the ferromagnetic layers staying relatively fixed when moderate magnetic fields are applied. However, in a pseudo spin valve, this fixed magnetization is a result of a relatively high switching field rather than a result of being pinned. For example, the fixed ferromagnetic layer may be made substantially thicker than the free ferromagnetic layer.

GMR devices, including spin valves and pseudo spin valves, can be used as data storage elements, i.e., "bits," in magnetic random access memory (MRAM) devices. In typical MRAM devices, the logical state of a GMR bit is based on its resistance, which, in turn, is based on the relative orientations of the magnetizations of the ferromagnetic layers. Thus, in one logical state, e.g., a "0" state, a GMR bit may have its ferromagnetic

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layers in a parallel orientation and, thus, may exhibit a low electrical resistance. In the other logical state, e.g., a "1" state, the GMR bit may its ferromagnetic layers in an antiparallel orientation and, thus, may exhibit a higher electrical resistance. Data may be written to a GMR bit by applying a magnetic field sufficient to change the magnetization of the "free" ferromagnetic layer, In this way, the "free" ferromagnetic layer functions as a "switching layer" that stores data in the form of a particular magnetization orientation relative to the other ferromagnetic layer, the "reference layer."

In general, the process for fabricating GMR bits involves depositing the ferromagnetic layers and other layers that make up the GMR device over one or more underlayers and etching the deposited layers to a desired configuration of GMR bits. Examples of such fabrication processes are described in U.S. Patent No. 5,496,759 and in U.S. Patent Application No. 10/284,922, filed October 31, 2002, which are incorporated herein by reference. However, there continues to be a need for improved methods of fabrication in order to improve yields and/or performance of GMR devices.

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SUMMARY

In a first principal aspect, the present invention provides a method of fabrication for a magnetoresistive device. In accordance with the method, an oxide layer is formed, a plurality of magnetoresistive device layers is formed above the oxide layer, and an etch stop is formed above the magnetoresistive device layers. The magnetoresistive device layers are surrounded with an oxygen barrier. The oxide layer is etched while the magnetoresistive device layers are surrounded by the oxygen barrier.

In a second principal aspect, the present invention provides a method of fabrication for a magnetic device. In accordance with the method, an oxide layer is formed, and at least one ferromagnetic layer is formed above the oxide layer. The at least one ferromagnetic layer is surrounded with a barrier to protect the at least one ferromagnetic layer from exposure to oxygen. The oxide layer is etched with the at least one ferromagnetic layer is surrounded by the barrier.

In a third principal aspect, the present invention provides a method of fabrication for a giant magnetoresistive (GMR) device. In accordance with the method, a silicon oxide is layer is formed, a first silicon nitride layer is formed on the silicon oxide layer, and a plurality of GMR device layers is formed on the first silicon nitride layer. The plurality of GMR device layers includes a plurality of ferromagnetic layers and a nonmagnetic layer. An etch stop is formed on the GMR device layers, and a second silicon nitride layer is formed on the etch stop. The GMR device layers are patterned to define sidewalls of the GMR device layers. The second silicon nitride layer is patterned

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to expose a portion of the etch stop. The sidewalls of the GMR device layers are covered with a photoresist layer. While the sidewalls of the GMR device layers are covered by the photoresist layer, the first silicon nitride layer and the silicon oxide layer are etched to expose at least one electrical contact.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic view of the layers of a spin valve, in accordance with an exemplary embodiment of the present invention;

Figure 2 is a schematic view of the layers of a pseudo spin valve, in accordance with an exemplary embodiment of the present invention;

Figure 3 is a schematic view showing a stage in the fabrication of a magnetoresistive device, in accordance with an exemplary embodiment of the present invention;

Figure 3A is a schematic view showing a stage in the fabrication of a magnetoresistive device, in accordance with an exemplary embodiment of the present invention;

Figure 4 is a schematic view showing a stage in the fabrication of a magnetoresistive device, in accordance with an exemplary embodiment of the present invention;

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Figure 5 is a schematic view showing a stage in the fabrication of a magnetoresistive device, in accordance with an exemplary embodiment of the present invention;

Figure 6 is a schematic view showing a stage in the fabrication of a magnetoresistive device, in accordance with an exemplary embodiment of the present invention; and

Figure 7 is a schematic view showing a stage in the fabrication of a magnetoresistive device, in accordance with an exemplary embodiment of the present invention.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

The present invention, in exemplary embodiments, provides methods for fabricating GMR devices, such as spin valves or pseudo spin valves, e.g., as magnetic bits for magnetic memories. In many applications, it is desirable to form the magnetic bits above a layer of silicon oxide, for example, to provide functionality and compatibility with standard fabrication processes. However, it has been found that the process of etching into the silicon oxide can release oxygen that, if allowed to come into contact with the metal layers in the magnetic bits, can degrade the performance of the GMR devices. The present invention addresses this problem by surrounding the magnetic bits with a barrier that protects the metal layers from exposure to oxygen while

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the silicon oxide layer is being etched. The oxygen barrier may include, for example, one or more photoresist layers and/or silicon nitride layers.

1. Exemplary Spin Valve And Pseudo Spin Valve Constructions

Figure 1 schematically illustrates the layers of an exemplary spin valve 10 that may be used in the present invention. It is to be understood that spin valve 10 may be formed on a substrate or on one or more other underlayers not shown in Figure 1. For example, spin valve 10 may be formed on dielectric materials, such as silicon nitride or silicon oxide. Thus, spin valve 10 may include a seed layer 12, formed atop another layer (not shown), in order to facilitate the formation of the metal layers above it in spin valve 10. In an exemplary embodiment, seed layer 12 is a metal such as tantalum. The thickness of seed layer 12 may range from about 1 to 10 nanometers, depending on the materials used. Thus, in a typical example, seed layer 12 may be about 5 nanometers of tantalum.

A first ferromagnetic layer 14 is formed on seed layer 12. Ferromagnetic layer 14 serves as the "free" or "switching" layer in spin valve 10. Ferromagnetic layer 14 includes a ferromagnetic material, such as iron, nickel, cobalt and/or alloys thereof, such as NiFe, CoFe, NiFeCo, and NiFe/CoFe. The thickness of ferromagnetic layer 14 may, for example, be between 0.1 and 10 nanometers. A nonmagnetic layer 16 is formed on ferromagnetic layer 14. Nonmagnetic layer 16 is a nonmagnetic conductor, such as copper, with a thickness, for example, in the range of 0.5 to 4 nanometers.

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A second ferromagnetic layer 18 is formed on nonmagnetic layer 16. Ferromagnetic layer 18 includes a ferromagnetic material, such as iron, nickel, cobalt and/or alloys thereof, such as NiFe, CoFe, NiFeCo, and NiFe/CoFe. The thickness of ferromagnetic layer may, for example, be between 0.1 and 10 nanometers. An antiferromagnetic layer 20 is formed on ferromagnetic layer 18. Antiferromagnetic layer 20 may include antiferromagnetic materials, such as FeMn alloys or PtMn alloys, and may have a thickness, for example, from 5 to 50 nanometers. Antiferromagnetic layer 20 pins the orientation of the magnetization of ferromagnetic layer 18. Thus, ferromagnetic layer 18 serves as the "pinned" or "reference" layer in spin valve 10.

Spin valve 10 may also include a cap layer 22 formed on antiferromagnetic layer 20. Cap layer 22 may include one or more layers provided for diffusion barriers, passivation, and/or in order to enhance the magnetoresistance of spin valve 10. In an exemplary embodiment, cap layer 22 may include a diffusion barrier consisting of a layer of tantalum about 1 to 5 nanometers thick. Spin valve 10 may also include other layers, depending on the particular application and/or method of fabrication. In addition, one or more other layers may be formed above and/or to the side of spin valve 10.

Figure 2 schematically illustrates the layers of an exemplary pseudo spin valve 30 that may be used in the present invention. The construction of pseudo spin valve 30 is similar to that of spin valve 10, except that no antiferromagnetic layer is included and the stacking of the switching and reference ferromagnetic layers is reversed. Thus, pseudo spin valve 30 may include a seed layer 32 to facilitate the formation of the metal layers of

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pseudo valve 30 above a dielectric layer, such as silicon nitride or oxide. Seed layer 32 may be about 5 nanometers of tantalum, for example. A first ferromagnetic layer 34 is formed on seed layer 32. Ferromagnetic layer 34 may serve as the fixed or reference layer in pseudo spin valve 30. Ferromagnetic layer 34 may include a material, such as Ni, Fe, Co, NiFe, CoFe, NiFeCo, and/or NiFe/CoFe, and may have a thickness, for example, between 0.1 to 10 nanometers. A nonmagnetic layer 36 is formed on ferromagnetic layer 34. Nonmagnetic layer 36 is a nonmagnetic conductor, such as copper, and may have a thickness in the range of 2.5 to 3.5 nanometers. A second ferromagnetic layer 38 is formed in nonmagnetic layer 36. Ferromagnetic layer 38 may serve as the free or switching layer in pseudo spin valve 30. Ferromagnetic layer 38 may include a material, such as Ni, Fe, Co, NiFe, CoFe, NiFeCo, and/or NiFe/CoFe, and may have a thickness, for example, between 0.1 to 10 nanometers. A cap layer 40 may be formed on ferromagnetic layer 38. Cap layer 40 may include one or more layers provided for diffusion barriers, passivation, and/or in order to enhance the magnetoresistance of pseudo spin valve 30. Cap layer 40 may, for example, include a diffusion barrier consisting of a layer of tantalum about 1 to 5 nanometers thick.

2. Exemplary Method Of Fabrication

Figures 3 through 7 illustrate several stages in an exemplary method of fabricating a magnetic bit, e.g., for a magnetic memory. Figure 3 illustrates a multilayered structure 100 that is ready to be patterned to define the configuration of the magnetic bit. In an exemplary embodiment, multilayered structure 100 includes a layer 102 of silicon oxide,

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e.g., SiO_2. Oxide layer 102 may be formed over one or more underlayers (not shown) that may include metal layers, semiconductor devices, and/or other circuitry. In an exemplary embodiment, oxide layer 102 includes about 2000 nanometers of PVD silicon oxide and about 1000 nanometers of CMP silicon oxide.

A first silicon nitride layer 104 is formed on oxide layer 102. In this example, first silicon nitride layer 104 is about 150 to 200 nanometers thick and is formed by PVD. First silicon nitride 104 may be provided as a spacer between oxide layer 102 and the magnetoresistive device layers above it, e.g., so that etching can extend below the level of the magnetoresistive device layers without immediately proceeding into oxide layer 102. First silicon nitride layer 104 may also serve as part of the oxygen barrier that protects the magnetoresistive layers from exposure to oxygen while oxide layer 102 is being etched, as described in more detail below.

Electrical contacts 106 may also extend through silicon oxide layer 102 and into silicon nitride layer 104. In an exemplary embodiment, electrical contacts 106 may comprise plugs of a conductive material, such as tungsten, filled into vias formed in silicon oxide layer 102 and may serve as electrical interconnects with metal layers, circuitry, or other layers below oxide layer 102.

Magnetoresistive device layers 108 are formed on first silicon nitride layer 104. In a preferred embodiment, magnetoresistive device layers 108 comprise the layers for a GMR device, such as a spin valve or a pseudo spin valve, and, thus, may be referred to herein as a "GMR stack." Thus, magnetoresistive device layers 108 may include the

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layers shown in Figure 1, for a spin valve, or may include the layers shown in Figure 2, for a pseudo spin valve. Magnetoresistive device layers 108 may be formed using one or more deposition techniques, such as chemical vapor deposition (CVD), low-pressure CVD (LPCVD), plasma vapor deposition (PVD), molecular beam epitaxy (MBE), sputtering, and/or ion beam deposition (IBD).

An etch stop 110 is formed on magnetoresistive layers 108. In a preferred embodiment, etch stop is titanium nitride (TiN). In an exemplary embodiment, the TiN layer is about 5 to 50 nm thick and may be deposited through low-temperature PVD. Alternatively, other materials, such as chromium silicon (CrSi), aluminum nitride (AlN), or tantalum nitride (TaN) could be used as etch stop 110.

A second silicon nitride layer 112 is formed on etch stop 110. Preferably, second silicon nitride layer 112 is thinner than first silicon nitride layer 104. Thus, in this example, second silicon nitride layer 112 may be about 10 to 100 nanometers thick. Second silicon nitride layer 112 may be formed by PVD, for example.

A photoresist layer 114 is formed on second silicon nitride layer 112 in order to pattern the magnetic bit. In an exemplary embodiment, as illustrated in Figure 3, ion milling is used for this patterning, with photoresist layer 114 serving as a masking layer. After ion milling, photoresist layer 114 is removed. Figure 4 shows the configuration multilayered structure 100 after ion milling and removal of photoresist layer 114. As shown in Figure 4, the ion milling defines sidewalls 116 of GMR stack 108, etch stop

110, and second silicon nitride layer 112. The ion milling may also extend partly into first silicon nitride layer 104.

Figure 3A illustrates an alternative approach to forming the construction shown in Figure 4. In this alternative approach, photoresist layer 114 is used as a masking to pattern second silicon nitride layer 112. After this patterning, photoresist layer 114 is removed. The patterned silicon nitride 114 layer, as shown in Figure 3A, is then used as a masking layer for the ion milling that results in the construction shown in Figure 4.

In the next stage, a third silicon nitride layer 118 may be formed on first silicon nitride layer 104 and second silicon nitride layer 112, as shown in Figure 5, e.g., to serve as a masking layer and to provide additional protection during subsequent etching. In an exemplary embodiment, third silicon nitride layer 118 is about 100 to 200 nanometers thick and is formed by a vapor deposition process, such as CVD or PVD. A photoresist layer 120 is formed on third silicon nitride layer 118 as a masking layer for further patterning to open electrical contacts to the magnetic bit.

In an exemplary embodiment, plasma etching, such as reactive ion etching (RIE), can be used for the patterning. The etching extends through third silicon nitride layer 118 and second silicon nitride layer 114 to expose electrical contact surfaces 122 on etch stop 110. The etching may also extend part of the way through first silicon nitride layer 102.

A photoresist layer 124 is then applied so as to surround silicon nitride layers 118 and 112, etch stop 110, and magnetoresistive device layers 108, as shown in Figure 6. In particular, photoresist layer 124 covers sidewalls 116 of magnetoresistive device layers

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108 and etch stop 110. In an exemplary embodiment, RIE is used to etch into silicon nitride layer 104 and silicon oxide layer 102 to expose electrical contacts 106. After this etching, photoresist layer 124 is removed. Figure 7 shows the configuration of multilayered structure 100 after this etching and removal of photoresist layer 124. In subsequent processing steps, one or more metallization layers may be deposited and etched to form electrically conductive pathways between magnetoresistive device layers 108 and electrical contacts 106.

It has been found that etching into silicon oxide layer 102 can release oxygen that can adversely affect the layers in or in proximity to the magnetic bit, including, for example, magnetoresistive device layers 108. Beneficially, however, the presence of photoresist layer 124 can substantially reduce the adverse affects of oxygen released during the etching into silicon oxide layer 102. In particular, photoresist layer 124 and first silicon nitride layer 104 together act as an oxygen barrier to protect the magnetic bit, including magnetoresistive device layers 108, from exposure to oxygen.

3. Conclusion

Exemplary embodiments of the present invention have been described above. Thus, references to specific thicknesses, materials, and fabrication methods are meant to be illustrative rather than limiting. Those skilled in the art will understand that changes and modifications may be made to these embodiments without departing from the true scope and spirit of the invention, which is defined by the claims.

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